# Damage Propagation Analysis of Electromechanical Actuator H-Bridge Power Stage

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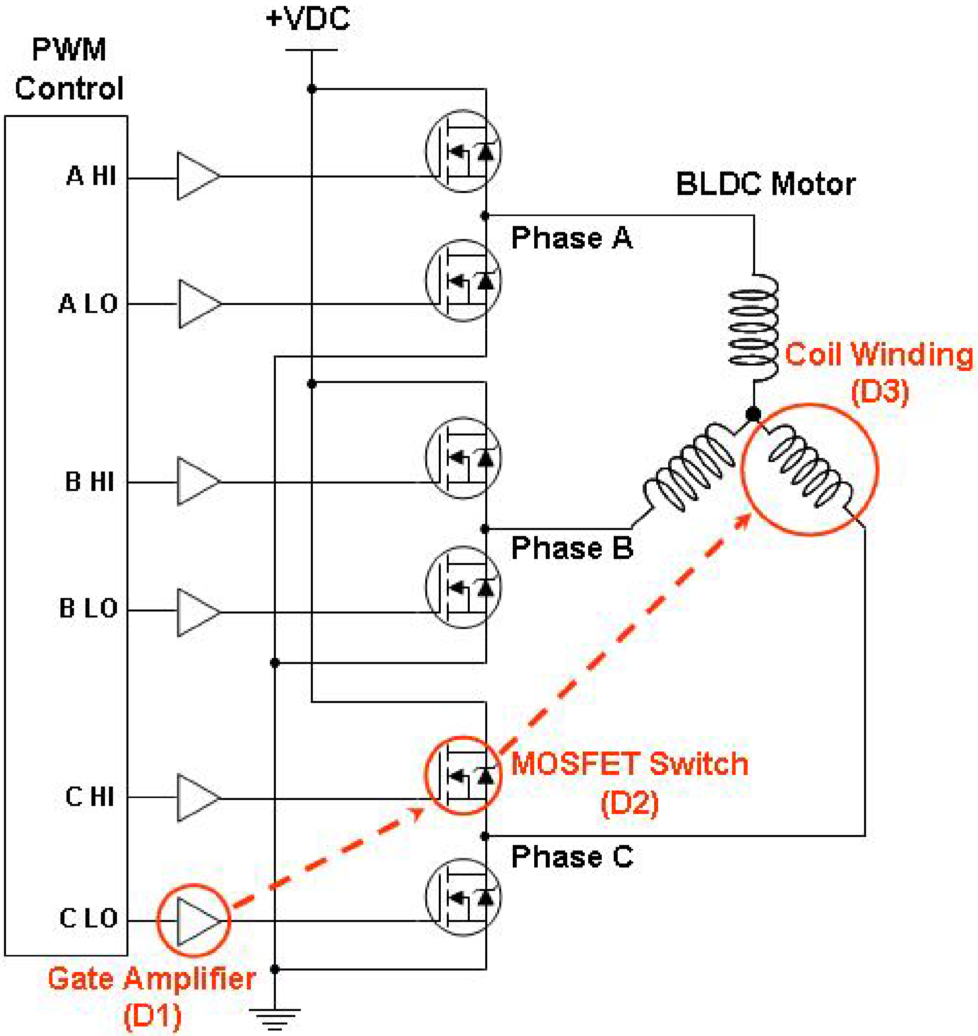
# Ridgetop Damage Propagation Methodology




- **Apply fault conditions to each critical component of the EMA H-Bridge, starting at the Gate Driver Amplifiers (D1) and progressing to the MOSFET Switches (D2) and Coil Windings (D3) of each BLDC motor phase**
- Conduct lab experiments to acquire and characterize the following error associated with each fault condition and resulting stress effect on down-stream components
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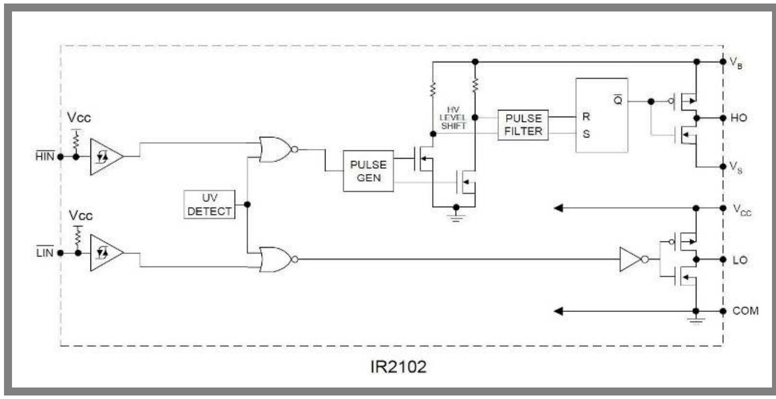
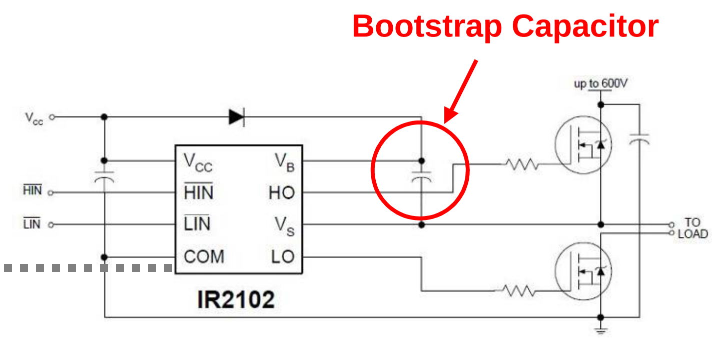
# H-Bridge Gate Driver Latch-up Failure

- Prevalent failure mode of gate driver IC is SCR latch-up of parasitic diode structures*
- Bootstrap configuration of gate driver common for high-power motor drive applications
- Gate driver latch-up may be exacerbated by degradation of bootstrap capacitor
- Test fixture constructed to duplicate latch-up failure on single phase of BLDC motor drive

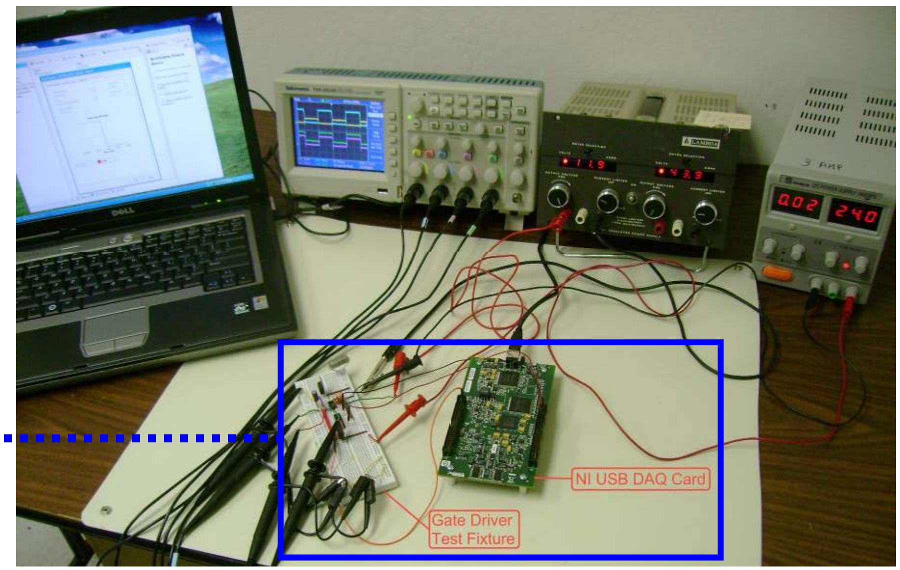
*International Rectifier Design Tip DT97-3

# Gate Driver Bootstrap Test Fixture

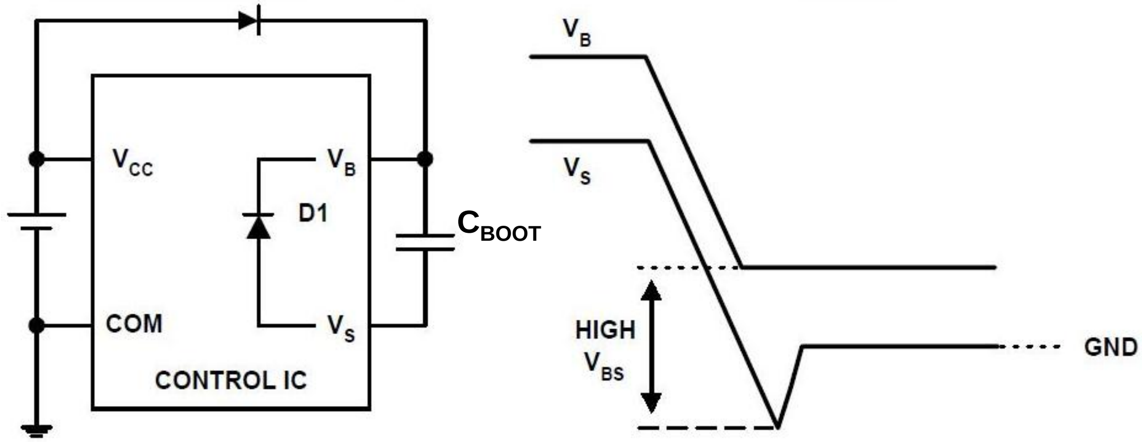



- ➢Gate Driver Test Fixture:
  - IR2102S Gate Driver IC
  - IRFZ44N Power MOSFETs
- ➢NI USB DAQ Card:
  - Bus Powered USB-6212
  - Driver LIN and HIN Control

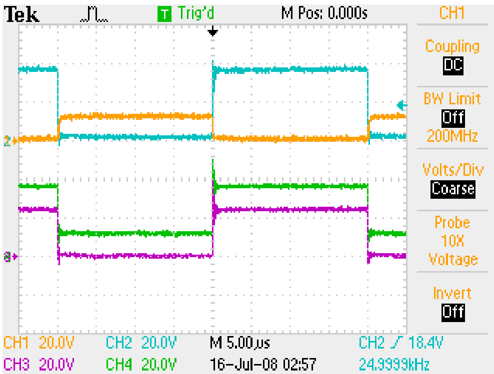


# $V_S$ Undershoot / $C_{BOOT}$ Overcharge

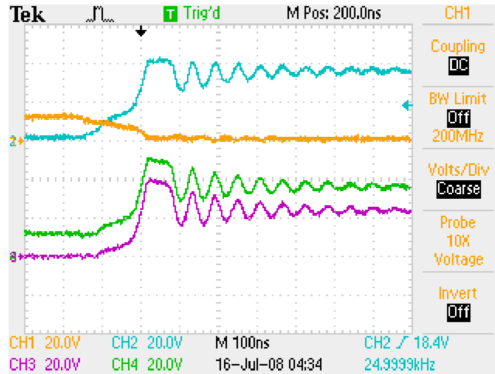



- Floating supply ($V_{BS}$) formed by bootstrap diode and capacitor is used to power high-side level shifter and gate driver
- High-side MOSFET switch turn-off events cause current flow in low-side freewheeling protection diode
- Diode voltage drop, along with stray low-side MOSFET switch inductance, pulls floating supply return node ($V_S$) below ground
- Excessive $V_S$ undershoot results in overcharging of $C_{Boot}$ and subsequent breakdown/latch-up of parasitic diode (D1)

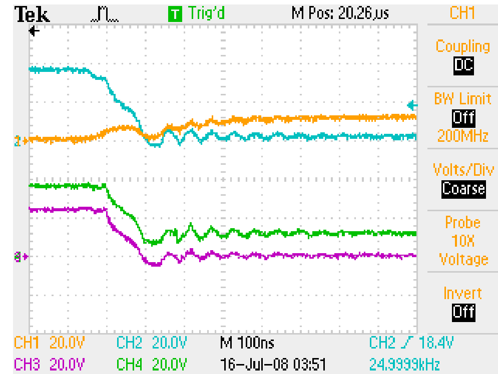
# Nominal vs. Degraded Bootstrap Capacitor



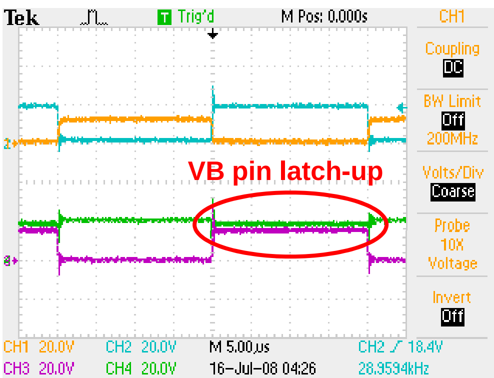
Nominal (0.5 μF)



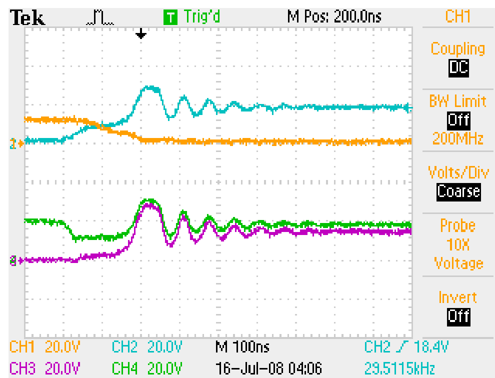
Rising Edge



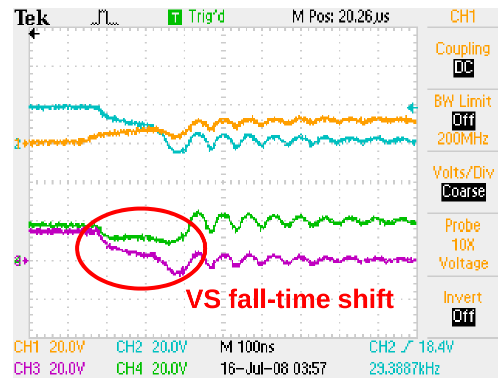
Falling Edge




Degraded (< 0.1 μF)



Rising Edge




Falling Edge

- LO (0..12V)
- HO (0..36V)
- VS (0..24V)
- VB (12..36V)

- **Gate driver circuit behavior with nominal vs. degraded bootstrap capacitor**
- **Latch-up observed on VB pin with bootstrap capacitance less than 0.1 μF**
- **Pronounced VS fall-time shift conducive to gate driver circuit prognostics**

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# Gate Driver Latch-up Failure Analysis

- Overcharging of bootstrap capacitor leads to latch-up of high-side gate driver output
- Bootstrap capacitor degradation reduces gate driver immunity to latch-up failure
- If latched off, gate driver malfunction is manifested in erratic BLDC motor operation
- If latched on, malfunction can lead to permanent MOSFET switch and/or gate driver IC damage

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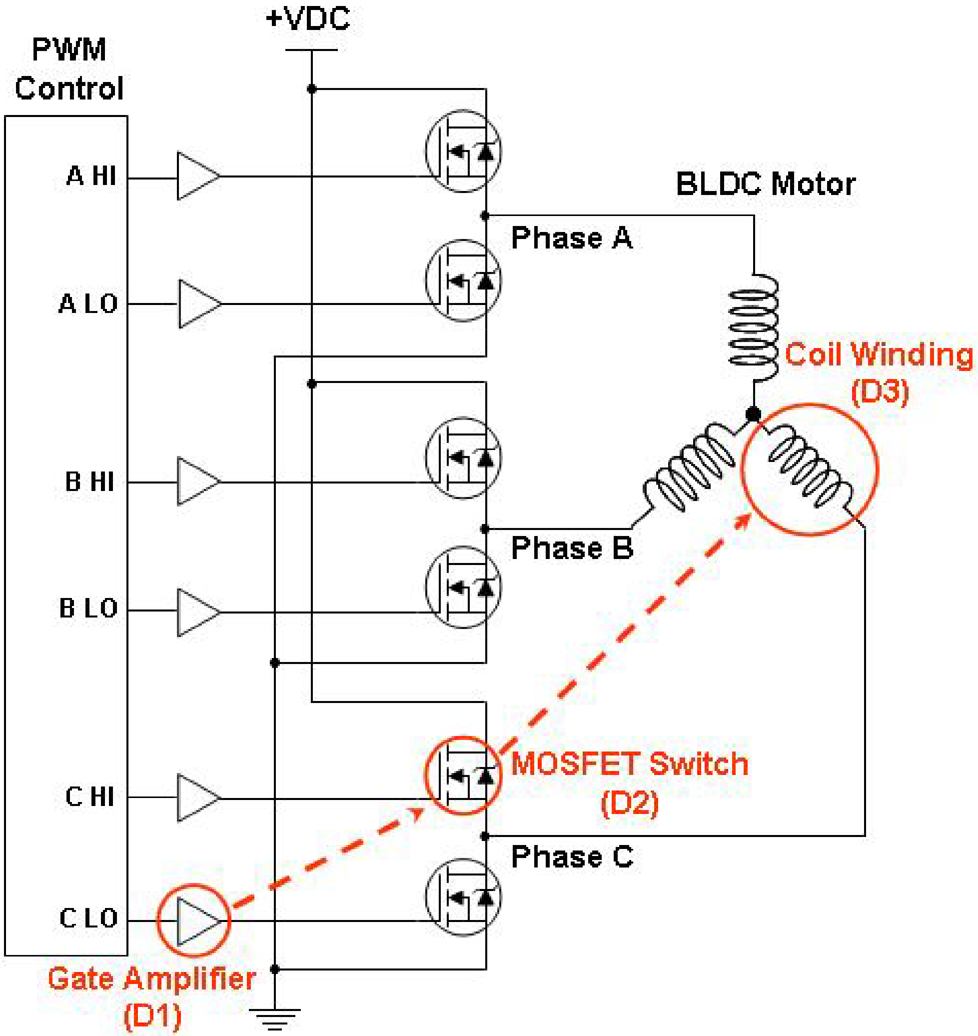


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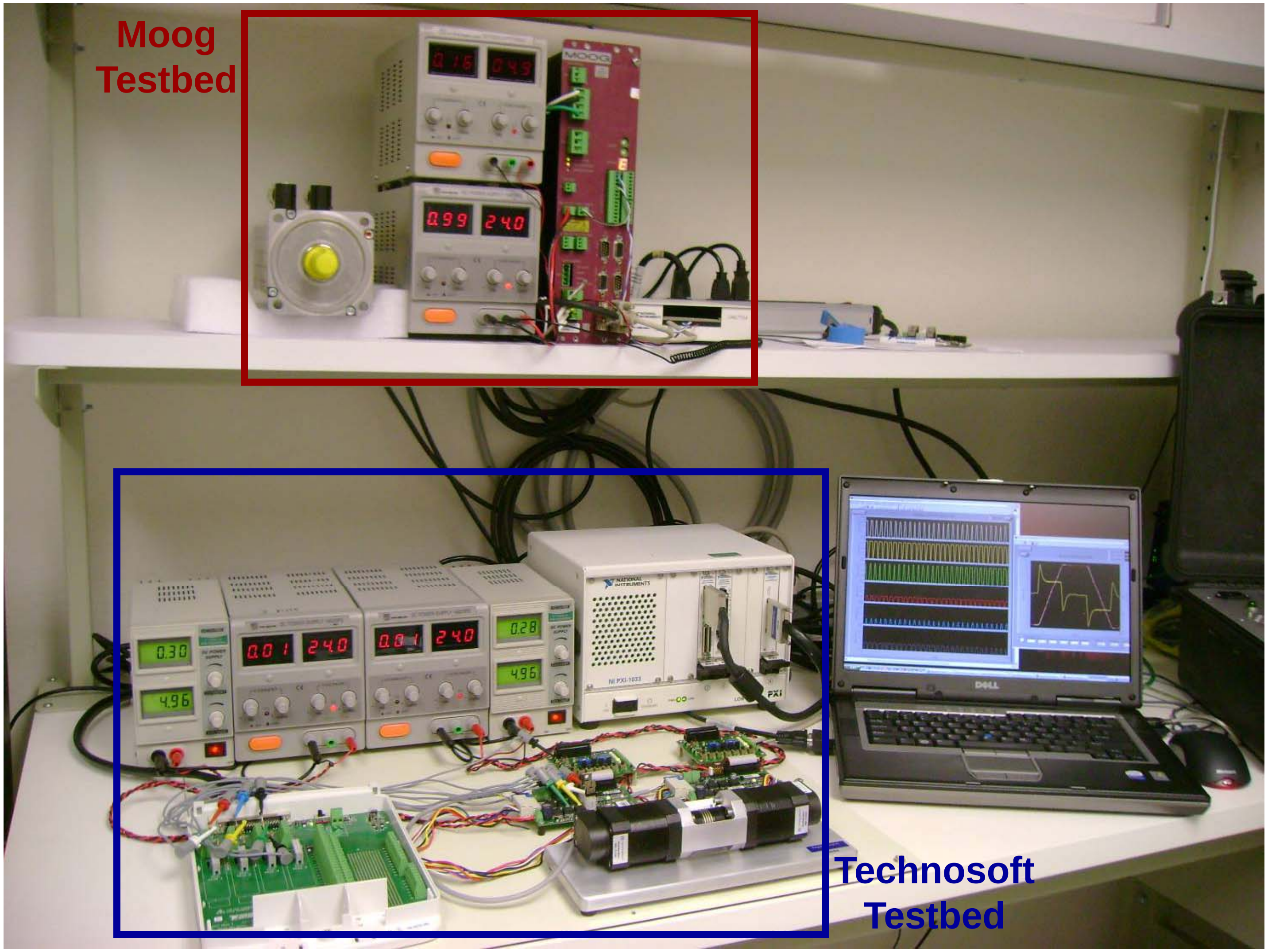
# Ridgetop Motion Control Laboratory

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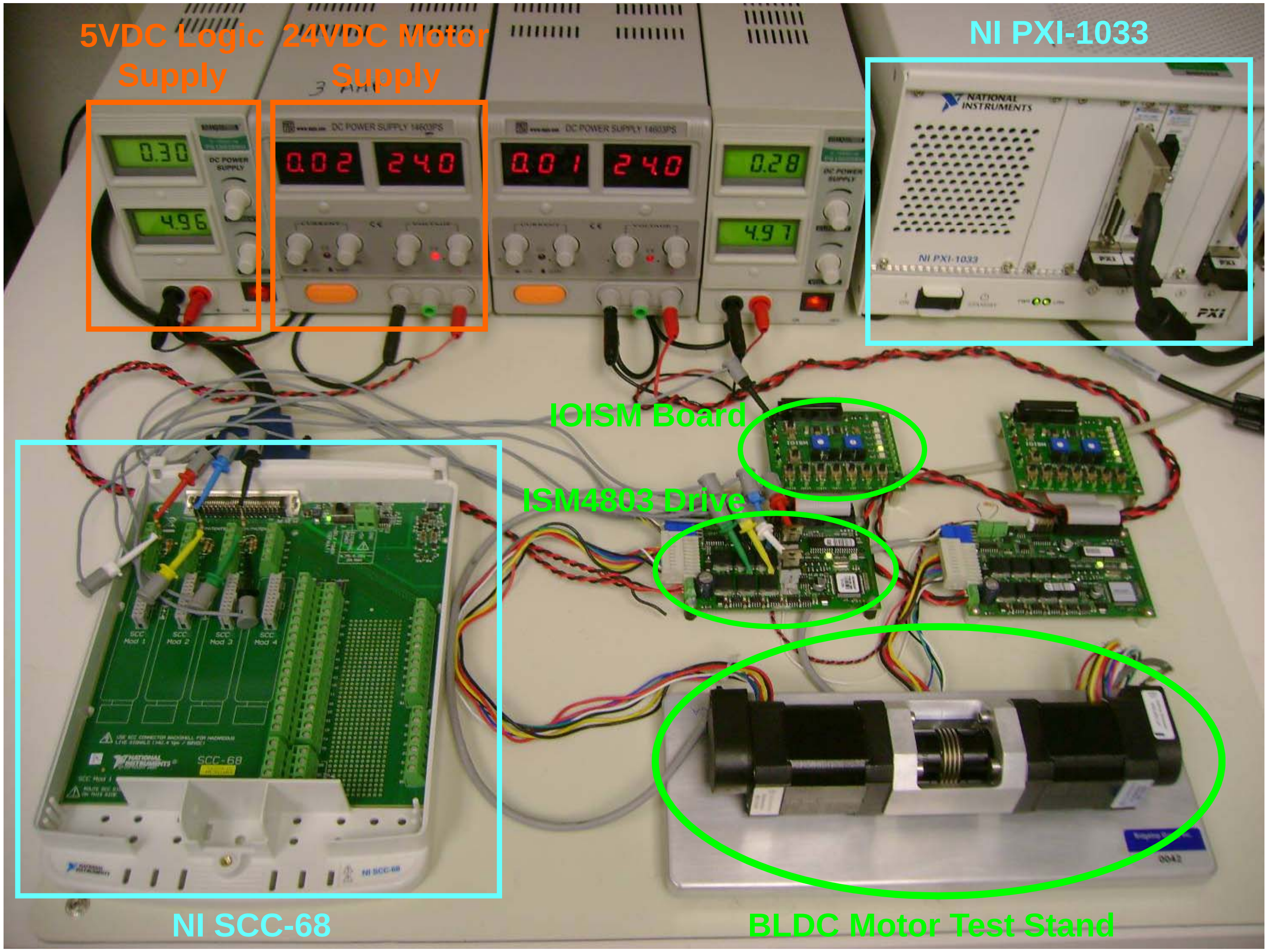
# Technosoft Testbed



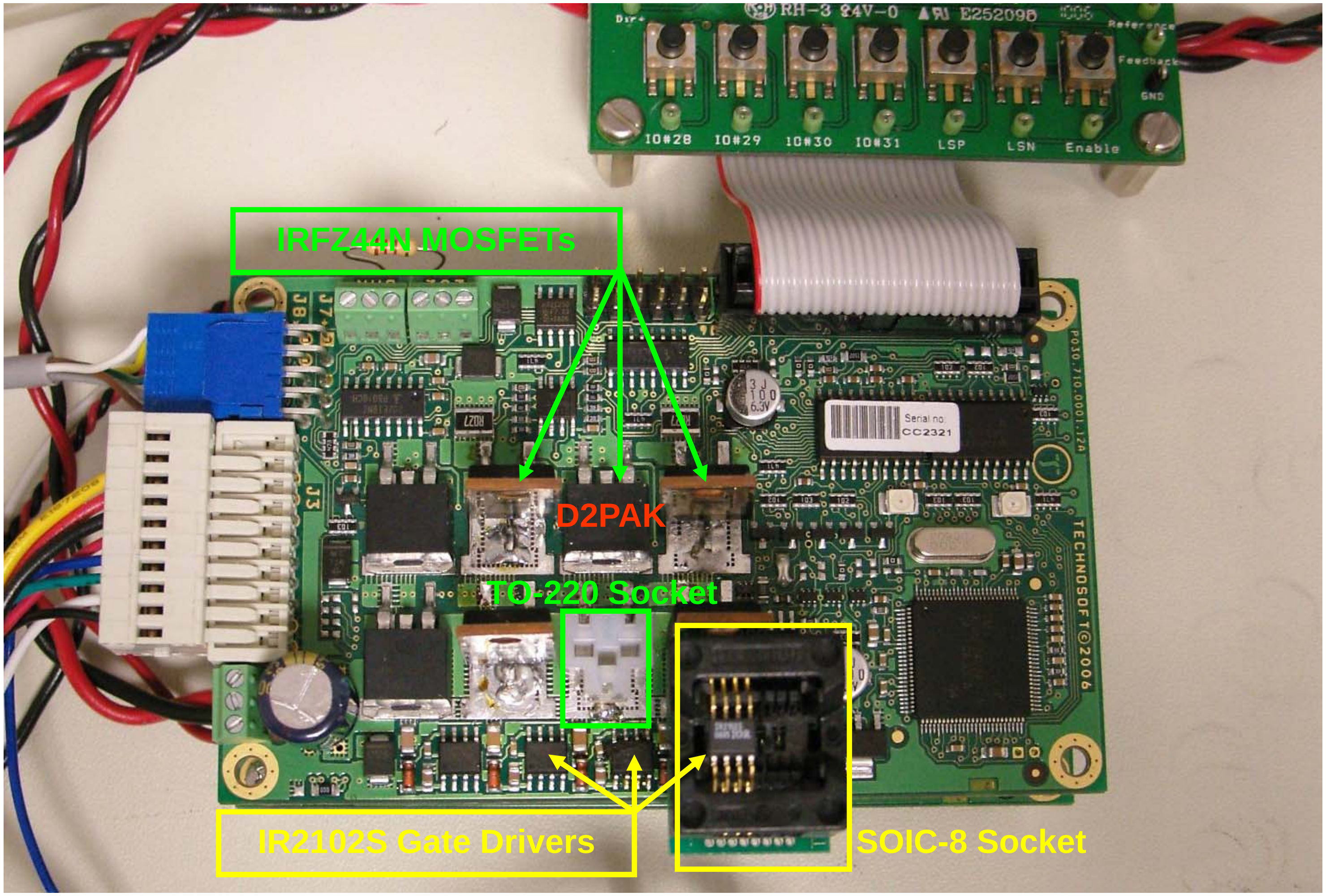
# H-Bridge Damage Propagation Experiment

- Modify Technosoft ISM4803 Servo Drive to facilitate H-bridge damage propagation experiments:
  - IRFZ44N D2PAKs replaced with TO-220 packages, i.e., form factor supported by ARC MOSFET aging lab
  - SOIC-8 socket installed to enable removal/replacement of IR2102S gate driver IC

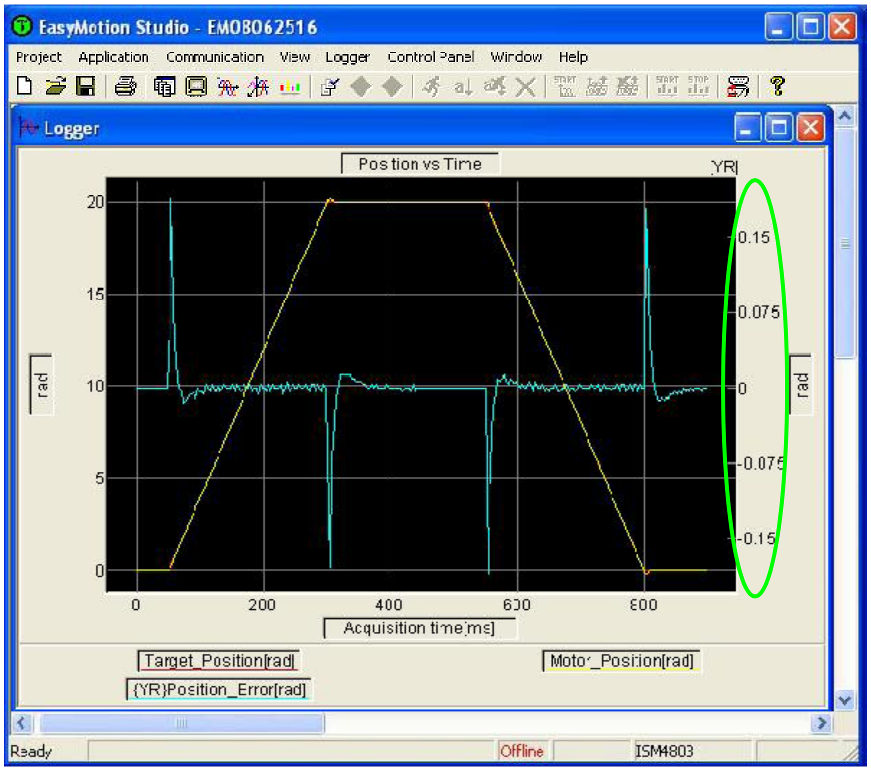
- Analyze effect of damaged gate driver circuit on low- and high-side MOSFET switches

- Correlate model parameters and simulation results with testbed

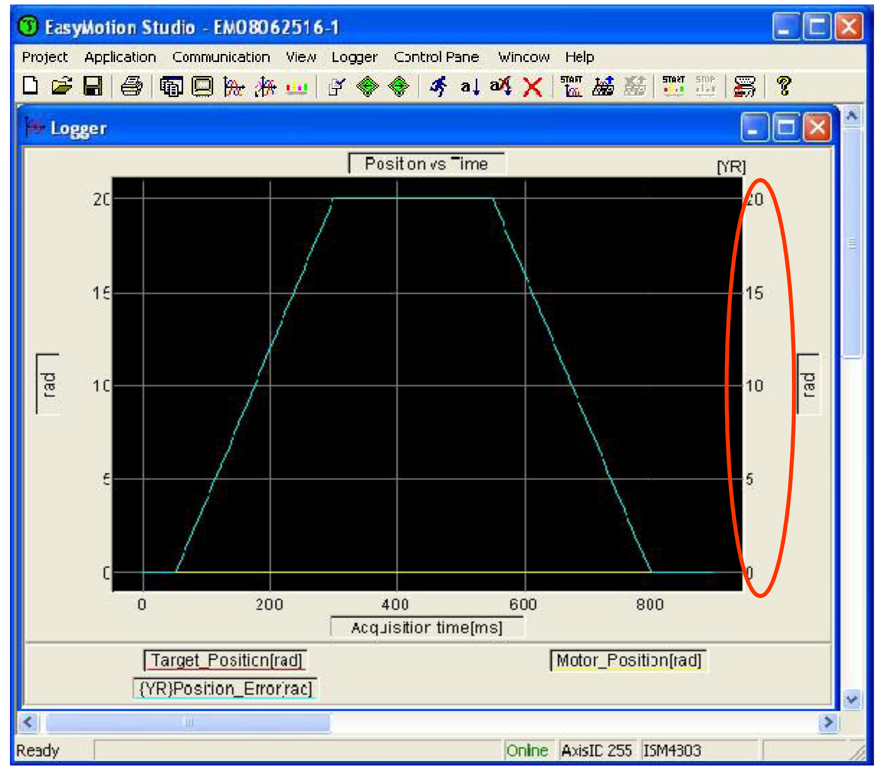
# Modified ISM4803 Servo Drive



# Testbed Results




Healthy Response - No Fault Present




Damage Response - Phase A MOFSETs Shorted

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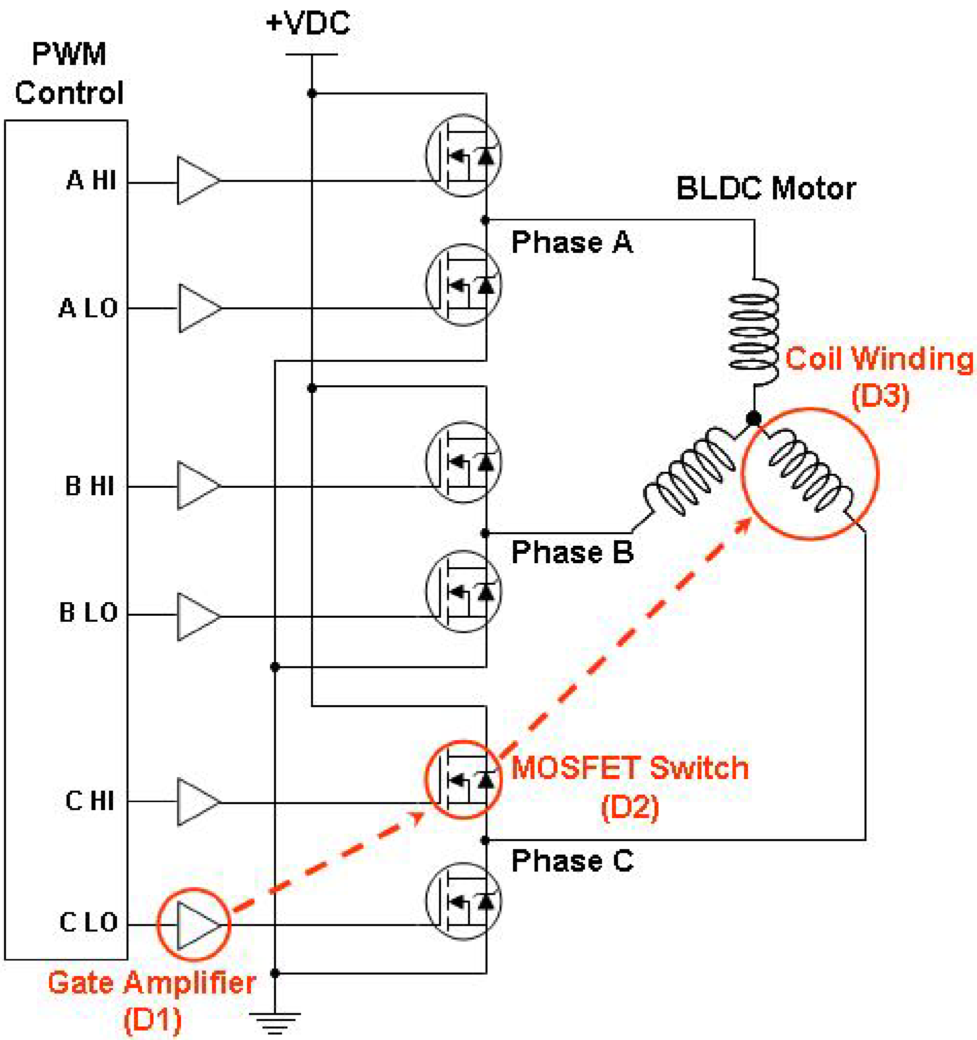


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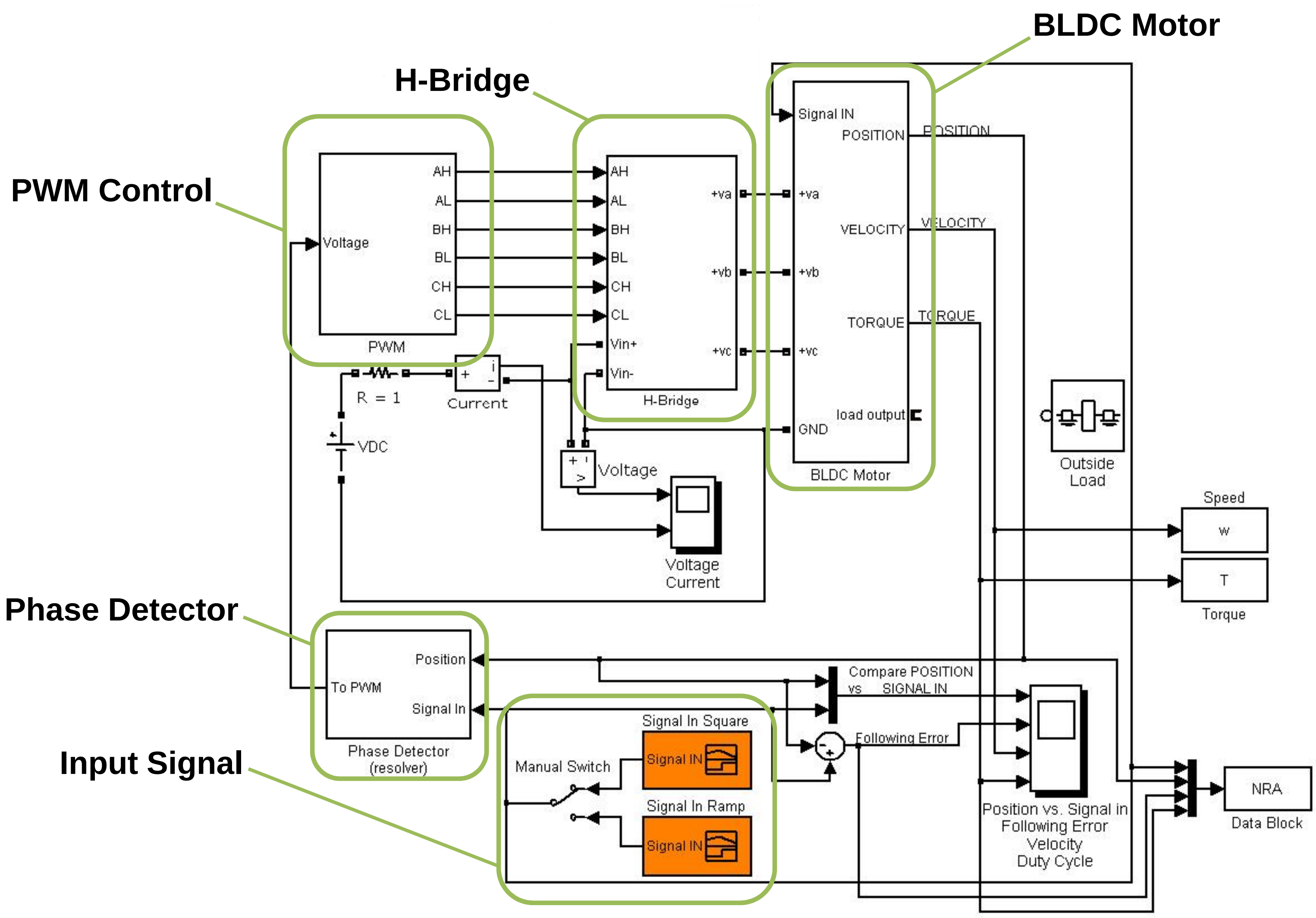
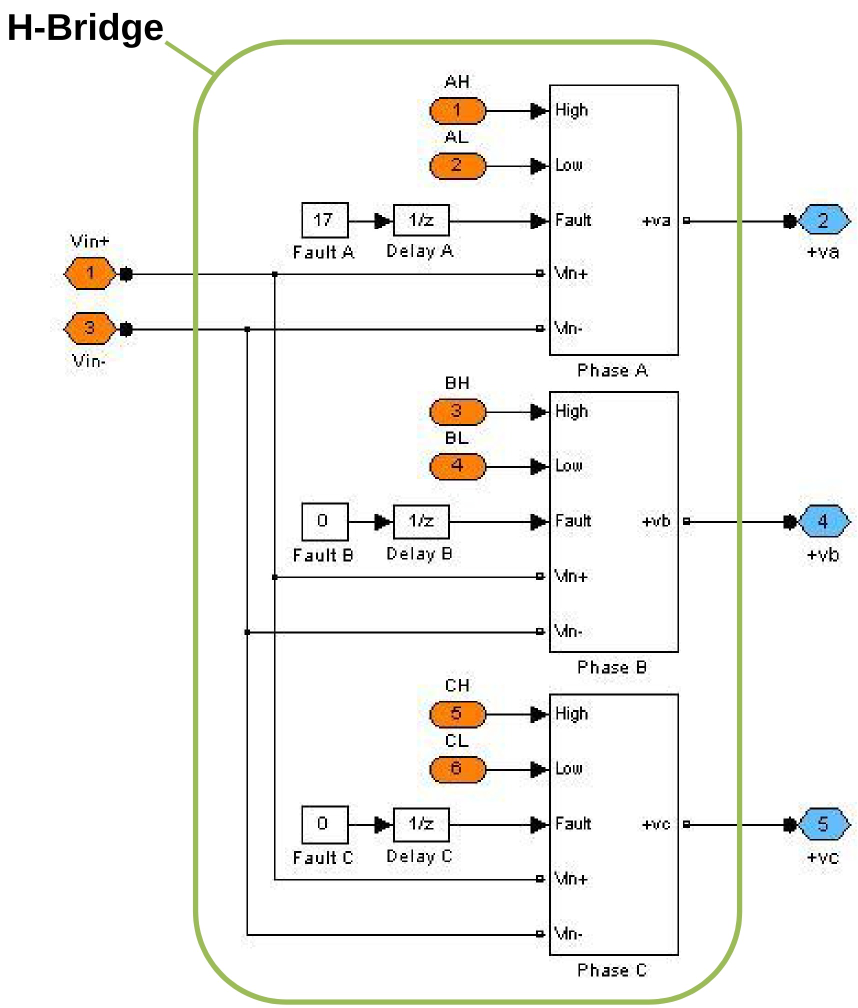
# Simulink Model



# MOSFET Open/Short Fault Injection




- For each phase, a packed fault code is composed by user and injected into model hierarchy through the H-bridge block
- Packed fault code is passed to both low- and high-side MOSFET switch blocks where it is decoded and executed

**Fault Decode:**
**Bit 0..3 = FL (Fault Low)**
**Bit 4..7 = FH (Fault High)**

**Fault Codes:**
**0 = NONE**
**1 = SHORT**
**2 = OPEN**

**FPACK = FH x 16 + FL**

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# Simulation Parameters / Fault Codes

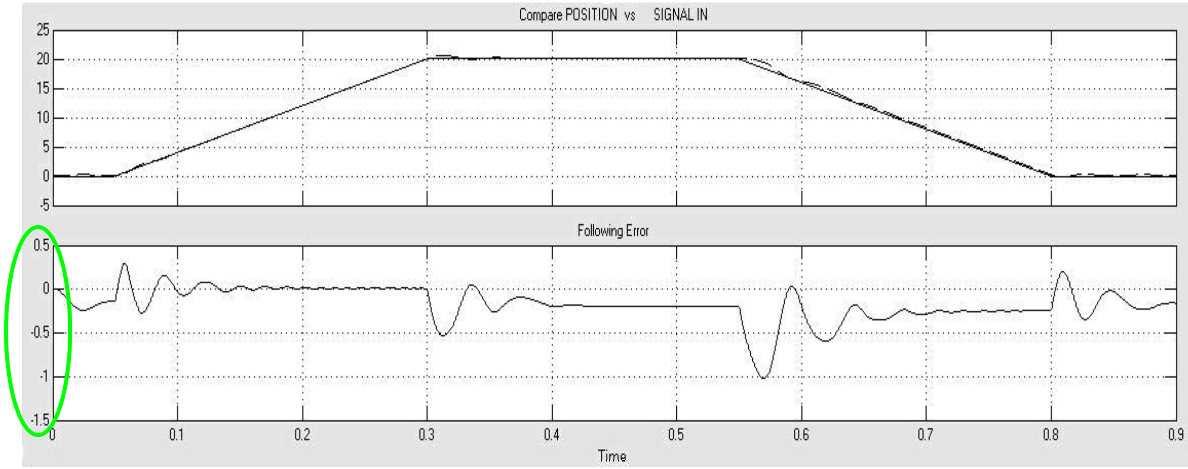
| Simulation Parameters* | |
|---|---|
| **Parameter** | **Value** |
| R = | 0.478 Ω |
| L = | 1.926 mH |
| Kemf = | 0.0355 Vrms/RPM |
| Kt = | 0.0355 Nm/A |
| B = | 0.00025 Nm/RPM |
| J = | 0.0000054 kg*m^2 |
| Jext = | N/A kg*m^2 |

| Fault Codes | |
|---|---|
| **Code** | **Description** |
| 00h | High-Side Normal, Low-Side Normal |
| 01h | High-Side Normal, Low-Side Short |
| 02h | High-Side Normal, Low-Side Open |
| 10h | High-Side Short, Low-Side Normal |
| 11h | High-Side Short, Low-Side Short |
| 12h | High-Side Short, Low-Side Open |
| 20h | High-Side Open, Low-Side Normal |
| 21h | High-Side Open, Low-Side Short |
| 22h | High-Side Open, Low-Side Open |

*Simulation parameters correlated with Technosoft testbed

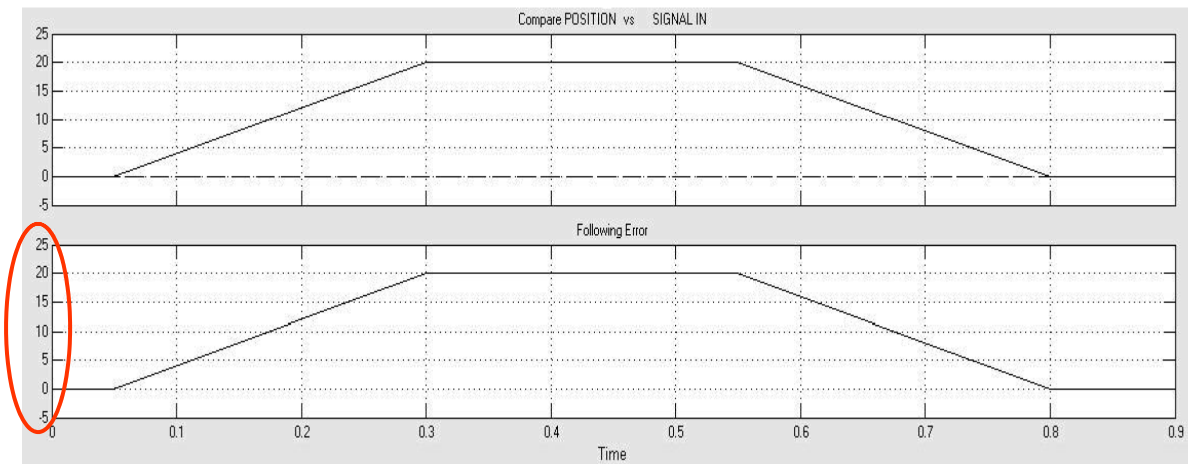
# Simulation Results

Minimal
Following Error
(radians)




**Healthy Response - No Fault Present**

Maximum
Following Error
(radians)




**Damage Response - Phase A MOFSETs Shorted**

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# H-Bridge Damage Propagation Analysis

- Gate driver amplifies TTL or CMOS PWM commutation signals to levels required to switch H-bridge MOSFETs
- Degradation and transient electrical/environmental conditions lead to gate driver open-circuit failures
- Open-circuit driver outputs leave both MOSFET gate inputs floating
- Floating gate inputs can cause both low- and high-side H-bridge switches to turn on simultaneously
- In resistive mode, MOSFETs are vulnerable to current impulses and drain-to-source short circuit damage

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# Thank You

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